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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/650,800	08/30/2000	Paul S. Neuman	RA 5290(33012/289/101)	1186

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EXAMINER
VITAL, PIERRE M

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 12/13/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/650,800	NEUMAN, PAUL S.	
	Examiner	Art Unit	
	Pierre M. Vital	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement filed December 18, 2000 complies with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Specification

2. The abstract of the disclosure is objected to because:

In line 7, after "requested", a word or term is missing.

Correction is required. See MPEP § 608.01(b).

3. The disclosure is objected to because of the following informalities:

(a) Although a reference to copending application appears in the first sentence of the specification, the Application Serial No. and filing date of the copending applications must also be included. Also, the current status of all non-provisional parent applications referenced should be included. See 37 C.F.R. 1.78 and MPEP § 201.11.

Appropriate correction is required.

(b) The disclosure uses terms such as "TLC", "UPI", "FLC-IC", "FLC-OC", and "SLC" which are not properly defined as required for acronyms. Acronyms must be defined at their first usage in the disclosure.

Appropriate correction is required.

(c) Please make corrections to the following terms:

On page 12, line 20, "ram" should be capitalized.

On page 13, line 3; replace "discusses" with –discussion--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for the purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language; or
>
> The publication under the treaty of an international application shall confer no rights and shall have no effect under this title other than that of a printed publication.
>
> The publication under the treaty defined in section 351(a) of this title, of an international application designating the United States shall be deemed a publication under section 122(b), except as provided in sections 102(e) and 154(d) of this title.
>
> Except as otherwise provided in this section, sections 4502 through 4504 and 4506 through 4507, and the amendments made by such sections, shall be effective as of November 29, 2000, and shall apply only to applications (including international applications designating the United States) filed on or after that date.

> The amendments made by section 4504 shall additionally apply to any pending application filed before November 29, 2000, if such pending application is published pursuant to a request of the applicant under such procedures as may be established by the Director.
>
> Except as otherwise provided in this section, the amendments made by section 4505 shall be effective as of November 29, 2000 and shall apply to all patents and all applications for patents pending on or filed after November 29, 2000. Patents resulting from an international application filed before November 29, 2000 and applications published pursuant to section 122(b) or Article 21(2) of the treaty defined in section 351(a) resulting from an international application filed before November 29, 2000 shall not be effective as prior art as of the filing date of the international application; however, such patents shall be effective as prior art in accordance with section 102(e) in effect on November 28, 2000.

5. Claims 1-3 are rejected under 35 U.S.C. 102(e) as being anticipated by Lynch et al. (US6,061,766).

As per claim 1, Lynch discloses a data processing system having a system bus {*i.e., common memory bus*} and having a processor with a level one cache memory {*i.e., CPU 302, on-board caches 308*} responsively coupled to a level two cache memory {*i.e., cache 306*} which is responsively coupled to a level three cache memory {*i.e., main memory*} [Fig. 3; col. 3, lines 36-43]; and having a circuit for Snooping said system bus [col.3, line 60]; and first logic which invalidates a corresponding level one cache memory location {*i.e., processor invalidate data in their own memories (or on-chip caches)*} in response to either a non-local write or write ownership request {*i.e., request for exclusive use*} [col. 1, lines 40-48, 53-55].

As per claim 2, Lynch discloses a second logic which inhibits said first logic from invalidating for mode 3 requests without ownership {*i.e., only requests for exclusive use which match cache tags are invalidated*} [Fig. 4; col. 4, lines 19-30].

As per claim 3, Lynch discloses third logic which invalidates said corresponding cache memory location in response to a SNOOP hit [Fig. 4; col. 4, lines 24-26].

As per claim 4, Lynch discloses fourth logic which retrieves and records data in response to a level one cache read miss and a level two cache memory read miss [Fig. 4, steps 408-420].

6. Claims 6 is rejected under 35 U.S.C. 102(e) as being anticipated by Arimilli et al. (US6,397,300).

As per claim 6, Arimilli discloses a data processing system comprising a level one cache memory {*i.e., CPU 150, L1 cache 200*}; a level two cache memory responsively coupled to said level one cache memory {*i.e., L2 cache 202*}; a level three memory responsively coupled to said level two cache memory {*i.e., main memory*} [Fig. 4, col. 8, lines 30–49]; and a first circuit to invalidate a corresponding portion of said level one cache memory in response to a level one cache memory write hit and a level two cache memory write {*i.e., if hit in upper level cache, cache line in upper level cache invalidated*} [col. 5, lines 12-25].

As per claims 11 and 16, Arimilli discloses a method of maintaining validity of data within a level one cache memory of a processor responsively coupled to a level two cache memory which is responsively coupled to a system memory bus [Fig. 4, *L1 cache 200, L2 cache 202, system bus 105*] comprising: formulating a write request {*i.e.,*

issuing store operation} [col. 12, lines 10]; first experiencing a level one cache memory miss in response to said write memory request [col. 12, line 18]; second experiencing a level two cache memory hit in response to said first experiencing step [col. 9, lines 33-34, col. 12, lines 54-56]; and invalidating a portion of said level one cache memory corresponding to said write memory request in response to said second experiencing step {*i.e., L2 cache controls update and invalidation of L1 cache*} [col. 10, line 45 - col. 11, line 19].

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lynch et al. (US6,061,766) and Hazawa (US4,891,809).

As per claim 5, Lynch discloses the claimed invention as detailed above in the previous paragraphs. However, Lynch does not specifically teach invalidating a level one cache memory in response to a level two cache memory generating a parity error as recited in the claim.

Hazawa discloses invalidating a level one cache memory in response to a level two cache memory generating a parity error [col.3, lines 38-48].

It would have been obvious to one of ordinary skill in the art, having the teachings of Lynch and Hazawa before him at the time the invention was made, to modify the system of Lynch to include invalidating a level one cache memory in response to a level two cache memory generating a parity error because it would have provided a cache memory having a normal error checking mode as taught by Hazawa by the provision of a sequential verification logic circuit for generating error indicating signals in sequence within the cache memory unit [col. 1, lines 30-37] as taught y Hazawa.

9. Claims 7-9, 12-14 and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli et al. (US6,397,300) and Lynch et al. (US6,061,766).

As per claims 7, 12 and 17, Arimilli discloses the claimed invention as detailed above in the previous paragraphs. However, Arimilli does not specifically teach a second logic which inhibits said first logic from invalidating for mode 3 requests without ownership.

Lynch discloses a second logic which inhibits said first logic from invalidating for mode 3 requests without ownership {*i.e., only requests for exclusive use which match cache tags are invalidated*} [Fig. 4; col. 4, lines 19-30].

As per claims 8, 13 and 18, Arimilli discloses the claimed invention as detailed above in the previous paragraphs. However, Arimilli does not specifically teach third logic which invalidates said corresponding cache memory location in response to a SNOOP hit.

Lynch discloses third logic which invalidates said corresponding cache memory location in response to a SNOOP hit [Fig. 4; col. 4, lines 24-26].

As per claims 9, 14 and 19, Arimilli discloses the claimed invention as detailed above in the previous paragraphs. However, Arimilli does not specifically teach fourth logic which retrieves and records data in response to a level one cache read miss and a level two cache memory read miss.

Lynch discloses fourth logic which retrieves and records data in response to a level one cache read miss and a level two cache memory read miss [Fig. 4, steps 408-420].

It would have been obvious to one of ordinary skill in the art, having the teachings of Arimilli and Lynch before him at the time the invention was made, to modify the system of Arimilli to include a second logic which inhibits said first logic from invalidating for mode 3 requests without ownership, logic which invalidates said corresponding cache memory location in response to a SNOOP hit, logic which retrieves and records data in response to a level one cache read miss and a level two cache memory read miss because it would have provided a snoop process for ensuring cache coherency and an increase in the hit rate of the system as taught by Lynch by invalidating a data object a data object contained in the on-chip cache and checking for

the presence of the data object in the on-chip cache [col. 2, lines 20-21, 34, 60-65] as taught by Lynch.

10. Claims 10, 15 and 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli et al. (US6,397,300) and Hazawa (US4,891,809).

As per claims 10 and 15, Arimilli discloses the claimed invention as detailed above in the previous paragraphs. However, Arimilli does not specifically teach invalidating a level one cache memory in response to a level two cache memory generating a parity error as recited in the claim.

Hazawa discloses invalidating a level one cache memory in response to a level two cache memory generating a parity error [col. 3, lines 38-48].

It would have been obvious to one of ordinary skill in the art, having the teachings of Arimilli and Hazawa before him at the time the invention was made, to modify the system of Arimilli to include invalidating a level one cache memory in response to a level two cache memory generating a parity error because it would have provided a cache memory having a normal error checking mode as taught by Hazawa by the provision of a sequential verification logic circuit for generating error indicating signals in sequence within the cache memory unit [col. 1, lines 30-37] as taught y Hazawa.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111 (c) to consider these references fully when responding to this action. The documents cited therein teach cache hierarchy, cache miss, cache invalidating and bus snooping.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre M. Vital whose telephone number is (703) 306-5839. The examiner can normally be reached on Mon-Fri, 8:30 am - 6:00 pm, alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-9000.

Reginald G. Bragdon
REGINALD G. BRAGDON
PRIMARY EXAMINER

Pierre M. Vital
December 10, 2002